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AN EXTERNALLY SYNCHRONIZED CLOCK FOR SATELLITE APPLICATIONS

by

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SUMMARY

This Report describes a system for synchronizing the output waveform of a clock with a pulse whose frequency is lower than that of the clock. It describes the system in general terms and details are given of an application in a satellite PCM data handling simulator. Suggested modifications for use in satellite applications are also described.

Departmental Reference: Space 304

CONTENTS

1 INTRODUCTION

During the development of a satellite PCM data handling simulator[1], it became necessary to develop a clock which could be synchronized from an associated computer being used to process the data. This need arose because the computer used could supply pulses only at the word rate, whereas the simulator also required pulses at the bit rate (in this particular case there are 8 bits per word).

It was realised that a similar requirement exists in satellites, where it is desirable to sample the data outputs of on-board scientific experiments at rates which are a function of the satellite spin rate. In such cases the synchronization pulses can be derived from sensors, e.g. sun sensors.

This Report gives details of a circuit arrangement that provides an equal mark to space ratio output waveform which is continuously variable from 80 pulses per second (pps) to 8000 pps. This corresponds to synchronization pulse frequencies of 10 pps to 1000 pps. However, considerable variations in system performance can be achieved by suitable modifications to the basic circuit and these modifications are discussed in section 4.

2 PRINCIPLE OF OPERATION

A block diagram is shown in Fig.1.

The clock consists essentially of a voltage controlled oscillator (VCO), whose output feeds a binary counter. The input voltage to the VCO is controlled by the difference between the time for a given number of counter output pulses and the time between successive input synchronization pulses.

The state of the binary counter is detected by two decoders and for the arrangement considered one decoder detects the 'all 1' state, and the other the 'all 0' state (although clearly any two states could be detected by appropriate design of the decoder logic). The VCO is gated 'ON' when the 'all 0' state is detected and remains 'ON' until the 'all 1' state is detected when the VCO is gated 'OFF'. The counter is reset to the 'all 0' state by the input synchronization pulse. The system is arranged for the counter to remain in the 'all 0' state for a time corresponding to the period of the VCO output waveform.

In addition to controlling the gating of the VCO the decoders select either a positive or a negative charging current for the input capacitor.

The 'all 1' decoder selects a positive charging current which decreases the VCO output frequency whereas the 'all 0' decoder selects a negative charging current increasing its frequency. The resultant frequency change depends upon the difference between the time the counter is in the 'all 1' state and the 'all 0' state. After a number of operating sequences this difference tends to zero and the VCO will have a continuous output slaved to the incoming synchronization pulses.

3 CIRCUIT DETAILS

3.1 General

The circuits described in this section are those developed for application in a satellite PCM data handling simulator. A circuit diagram is shown in Fig.2a and input and output waveforms in Fib.2b. Modifications to this basic arrangement to make it suitable for spacecraft applications are discussed in section 4.

3.2 The voltage controlled oscillator (VCO)

The requirements of the VCO are:

(i) An output frequency variable from 80 pps to 8000 pps in order to accept a wide range of bit rates.

(ii) A high input impedance so that the discharge rate of the input capacitor is negligible.

(iii) Output voltage levels and impedance compatible with the input requirements of the logic circuits used (in this case Series 74).

(iv) An output waveform period proportional to the input voltage. (This ensures the same system sensitivity over the required range of output frequencies.)

(v) An output voltage level consistent with the beginning of a pulse period when the VCO is gated on.

(vi) Self-starting capability with no allowance permitted in the number of output pulses before achieving a fixed frequency output.

A simple astable multivibrator was considered initially but was found to be inconsistent with (iv) above.

The circuit finally developed is shown in Fig.2a. It uses a comparator amplifier, μA 709C, whose output switches rapidly from a positive to a negative voltage when the voltage on capacitor C2 exceeds that on capacitor C1.

This transition triggers a monostable which turns on transistor T1. The period of the monostable (determined by C5 R20) is sufficiently long to completely discharge C2. On completion of this period, T1 is switched off, C2 charges through resistor R13 and the cycle is repeated again when the voltage across C2 exceeds that across C1. Thus the period of oscillation is determined by the voltage on C1, and provided the maximum period of oscillation is not greater than the time constant C2 R13 then the condition specified in requirement (iv) is adequately satisfied.

3.3 The binary counter

This is a four stage binary counter consisting of four bistables and associated control gates. The 'all 0' condition is obtained by feeding the synchronization pulses to the 'CLEAR' input of each bistable. These pulses are routed via logic gates because a direct connection would permit a situation whereby the circuit would fail to oscillate. With reference to Fig.2a, consider the situation when the supply voltages are first switched on. It is possible that the voltage on C1 is negative with respect to zero potential which produces a negative voltage at the comparator output (regardless of the voltage on C2) and inhibits the monostable. To overcome this condition the output of the monostable, normally at a logic '0' is now a logic '1', and is used to steer the incoming sync pulses through the gates to the 'PRESET' inputs of the bistables instead of the 'CLEAR' inputs. Thus the bistable outputs are set to the 'all 1' state which allows capacitor C1 to be charged from the positive current source. This positive charging will continue until the voltage on C1 is more positive than that on C2, when the comparator output voltage will become positive thereby creating the conditions required for the circuit to oscillate.

3.4 The decoders

The decoders are two four-input positive 'Nand' gates detecting the two required states. The output of the 'all 1' decoder is inverted to achieve correct operation of the positive constant current source.

3.5 The input capacitor

The purpose of the input capacitor C1 is to maintain the VCO input voltage (and therefore the output frequency) constant between successive charging periods. This voltage will change however due to:

(i) the comparator input current,

(ii) the leakage current of the constant current sources,

(iii) the leakage current due to the imperfections of the capacitor itself.

Therefore the larger the ratio of $C1/I_t$ (where I_t is the total leakage current) the smaller the voltage change at the VCO input.

It should be noted that since I_t includes the leakage current on capacitor C1 (possibly the dominant contribution), increasing the value of C1 does not necessarily increase $C1/I_t$.

The input capacitor chosen for the PCM simulator applications was a 12·5 μF non-polarised, wet electrolyte, tantalum foil type, having a maximum leakage of 2·5 μA at 20°C.

The maximum input current to the comparator amplifier is 1 μA and since other leakage currents are negligible, I_t max is 3·5 μA. Thus the VCO input voltage changes at a maximum rate of 280 mV/sec, and since the minimum frequency of the synchronization pulse is 10 pps (i.e. a pulse period of 0·1 sec) the maximum change in the VCO input voltage is 28 mV. This will cause a maximum variation in output frequency, between successive synchronization pulses of 0·56% which is readily acceptable for the PCM simulator application.

It should be noted that because the period of the VCO output is approximately proportional to the input voltage, this error is almost constant throughout the frequency range of input synchronization pulses.

3.6 The constant current sources

3.6.1 General

A constant current is supplied to capacitor C1 through either of the resistor transistor combinations T4 R11 or T5 R12 (see Fig.2a). The base currents for transistors T4 and T5 are supplied through the resistor transistor combinations of T2 R8 and T3 R9 respectively; and are negligible compared with the current through the resistor chains R8 R7 and R9 R10. Thus the base and emitter potentials of transistors T4 and T5 are well defined. The charging current I is determined by the relationship:

$$I = \pm\left[\frac{12 - V_b - V_{BE}}{10} - I_b\right] \text{ mA}$$

where V_b is the potential at the base of either T4 or T5

V_{BE} is the emitter base voltage of T4 or T5

I_b is the base current.

For the circuit configuration shown in Fig.2a the charging current is 0·7 mA.

3.6.2 Determining the value of charging current

Any error in VCO output frequency is corrected by the synchronization pulse because this error results in a time difference between the 'all 1' and the 'all 0' states. If this error is due to leakage currents causing the input capacitor to lose its charge, correction is required every synchronization pulse, which results in a constant time difference between the 'all 1' and the 'all 0' state. To make this difference small the charging current should be made large but there is a maximum value which if exceeded will prevent synchronization.

A design constraint is that the 'Error correction factor' should be less than 2, where 'Error correction factor' is defined as:

$$\frac{\text{The voltage change at the VCO input caused by the correction}}{\text{The original error in the VCO input voltage}}$$

The 'error correction factor' is proportional to the charging current and can be calculated using the relationship:-

$$\frac{I_c}{C1} \times \frac{t}{V}$$

where I_c is the charging current (μA)

C1 is the value of the input capacitor (μF)

t is the time between synchronization pulses (second)

V is the required value of the VCO input (volt).

For the circuit configuration shown in Fig.2a when operating at its minimum synchronization pulse repetition rate of 10 pps

$$t = 0{\cdot}1 \text{ sec}$$

$$V = 5 \text{ V}$$

$$C = 12{\cdot}5\,\mu\text{F}$$

$$I = 0{\cdot}7 \text{ mA}$$

resulting in an 'error correction factor' of 1·12.

3.7 System errors

3.7.1 General

Errors in the output waveform can be considered in terms of position errors or width errors or both. These errors are illustrated in Fig.3.

3.7.2 Position errors

It has previously been stated that because of leakage currents the output frequency of the VCO changes between successive synchronization pulses, whereupon a correction is applied. This change implies an increasing error in the position of the edges of successive output pulses, and can be expressed in terms of the time for a given number of output transitions, TO, and the time between successive sync pulses, TS:

$$\text{percentage error} = \left(\frac{TO}{TS} - \frac{NO}{NT}\right) \times 100$$

where NO is the number of output transitions considered

NT is the total number of transitions to fill the counter.

3.7.3 Width error

The time that the counter is in any one state will vary due to position errors. The time that the counter is in the 'all 1' state (TF) is determined by the combined width errors of all the previous states. Thus the maximum error can be expressed:

$$\text{percentage error (maximum)} = \left(\frac{TF \times NT}{TS} - 1\right) \times 100 \text{ .}$$

It should be noted that an error in matching the negative current source to the positive current source, will affect the width error of the 'all 1' state.

The circuit arrangement of Fig.2a gives position and width errors of less than 2%. Since this magnitude of error was acceptable for the simulator application no attempt was made to modify the circuit. However, such an error may well be unacceptable in spacecraft applications, and therefore some limited development was carried out with a view to minimising the sources of error.

4 FURTHER DEVELOPMENTS FOR SATELLITE APPLICATIONS

4.1 General

The system described in the previous section is unsuitable for satellite applications for three main reasons:

(a) The components chosen would have to be compatible with the low power consumption and high reliability criteria applied to all satellite electronic systems.

(b) The synchronization pulses may be generated only one per satellite revolution, which results in sync pulse repetition rates as low as 6 pulses per minute, and typically 30 pulses per minute. This compares with 10 pps to 1000 pps for the system previously described.

(c) The number of counter states in the existing system is 16, which would permit data sampling rates of only $\frac{10}{16}$ samples per second relative to a satellite spin rate of 6 pulses per minute. Required sampling rates are typically in the range 50-500 samples per second; and thus an increase in the number of counter stages for satellite applications is required. Furthermore, the clock is required to generate the bit rate which is typically 8 times faster than the sampling rate. It may also be desirable to generate a clock rate for the operation of an analogue-to-digital converter which is much greater than the data bit rate.

Possible modifications to the basic system to satisfy the satellite requirements are discussed in the following sections.

4.2 Decreasing the power consumption

The system described in section 3 consumes approximately 400 mW of power. The majority of this power is consumed by the logic and comparators, 270 mW and 100 mW respectively. Thus significant savings in power consumption will result from using low power logic and a more suitable comparator.

Using SN 54L logic units and a LM 101 amplifier operating from ±5 V voltage supplies the total power consumption is reduced to 77 mW.

4.3 Synchronization pulse repetition rate

Errors associated with the discharge of the input capacitor will increase as the time between consecutive synchronization pulses increases. The discharge rate is dependent upon the ratio $C1/I_t$ (section 3.5), and the aim must be to achieve a maximum value for this ratio consistent with acceptable component size. Two alternatives were considered.

(i) A solid tantalum capacitor, which has a good volumetric efficiency but a relatively high leakage current (e.g. the Kemet type K100A30 has a value of 100 μF, a volume of 0·076 in^3 and a maximum leakage current of 0·5 μA at 70°C operating at 5 V).

(ii) A metallized polycarbonate capacitor, which is relatively large for a given capacitance value but has a lower value of leakage current (e.g. STC type 43-16-ASA has a value of 4·7 μF and a volume of 0·346 in^3 and a maximum leakage current of 0·008 μA at 70°C operating at 5 V).

Using the solid tantalum type and introducing some minor modifications to the existing system position errors can be reduced to less than -0·5%. Using the other type of capacitor and more extensive modifications, the position error can be reduced to less than -0·2%. (Errors are calculated assuming a synchronization pulse repetition rate of 6 pulses per minute.)

Further error reductions can be achieved at the expense of circuit complexity, e.g. selecting resistor values to balance the various leakage currents and using thermistors to provide some degree of temperature compensation.

Another approach is to accept the relatively high leakage current of the tantalum capacitor, and attempt to compensate for it during the period between sync pulses. This can be achieved by replacing the capacitor C1 by a π network (Fig.4). By suitable choice of R and provided the resultant time constant is relatively large compared with the sync pulse period, it is possible to significantly reduce changes in VCO input voltage during this time.

The problems due to leakage at the VCO input can be eliminated by replacing the input capacitor and the current sources with a digital-to-analogue converter (DAC).

The inputs to the DAC could be from an 'up down' counter, the count decreasing during the first state of the main binary counter and increasing during the last state. The clock for the 'up down' counter can be supplied from a free-running astable.

However, system complexity is considerably increased and becomes comparable with an all digital system[2] and therefore has no advantages.

4.4 Number of counter states

The need for an increase in the number of counter states between synchronization pulses has already been discussed (4.1(c)), the upper limit being dependent upon the maximum operating frequency of the VCO. In the system described previously this was approximately 100K pps. Thus the maximum number of states for a maximum satellite spin rate of 30 pulses per minute is 200 000. An 18 stage binary counter gives a maximum of 262 144 states, which can be reduced to 200 000 by appropriate design of the decoder. However having a long binary counter reduces the time for which the current sources are switched on. This in turn increases the time required for initial synchronization and makes it more difficult to follow changes in synchronization frequency. It is expected that the latter difficulty will arise if the period between successive synchronization pulses (TS) changes by more than TS/NT, (where NT is the total number of counter states).

To overcome these difficulties two possible alternatives were considered: either the decoder can be made to combine a greater number of output states, thereby increasing the times for which the current sources are switched on, or the system can be modified to include a sync bistable (Fig.5) which is triggered by each incoming sync pulse. When the sync bistable 'OUTPUT' changes to a binary 0 the counter is cleared and the initial conditions set for the VCO. In this arrangement the decoders are replaced by coincidence gates which are operated by the 'OUTPUT' and $\overline{\text{'OUTPUT'}}$ of the sync bistable, and counter full bistable (Fig.5). The $\overline{\text{'OUTPUT'}}$ of the latter switches to a binary '1' when the counter is full. Thus, if the counter is filled before the arrival of a sync pulse, the positive current source is turned on, which increases the voltage on C1, and decreases the output frequency. This capacitor will continue to charge until the arrival of a sync pulse, when the sync bistable changes state, (the $\overline{\text{'OUTPUT'}}$ becoming a binary '0') thereby switching off the positive current source. The 'counter full' bistable will not change state until the sync bistable is triggered again, resetting the counter. However, if over compensation occurs the sync bistable is triggered before the counter full bistable changes

state, and conditions now exist whereby the negative current source is turned on. This causes a decreasing voltage on C1 which will continue until the counter full bistable changes state.

Thus, there is a gradual adjustment of input voltage (and hence output frequency) at each alternate sync pulse, until precise synchronization is achieved.

If only two or four states between synchronization pulses are required, it may be simpler to use 'frequency doubling circuits' as shown in Fig.6.

The sync pulses are used to trigger a bistable (sync bistable) whose output is a square wave, which is connected to the input of the frequency doubling circuit. The input waveform is integrated by R1 C1, smoothed by R2 C2, and the resultant waveforms A and B (Fig.6) are connected to the inputs of the comparator amplifier. The output of the comparator (waveform C) is a square wave having the same frequency as the input but leading by 90°. By connecting the outputs of the sync bistable and the comparator to the inputs of an 'exclusive OR gate' a waveform twice the frequency of the input is obtained.

This output can supply another similar circuit, whose output frequency will be twice that of the input sync pulses. Thus, four states are obtained between successive input sync pulses.

5 CONCLUSIONS

A clock generator capable of being synchronized from an external source having a variable pulse repetition frequency has been described. Although the system has been designed for a particular ground based test equipment, it has potential applications in spacecraft. Necessary modifications to the basic system for such an application are discussed and it is estimated that a clock generating frequencies in the range, a few pulses per minute to 1 MHz can be synchronised to an input waveform whose frequency may be varying and may be as low as a few pulses per minute.

Variations in the clock output frequency can be maintained better than 0·1%.

REFERENCES

No.	Author	Title, etc.
1	P. H. Clarkson	A satellite PCM data handling simulator. R.A.E. Technical Memorandum to be issued
2	W. C. Bartley et al	A digital system for accurate time sector division of a spin stabilised vehicle IEEE transactions on aerospace and electronic systems. Vol. AES-3 No.2 March 1967

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Fig 1

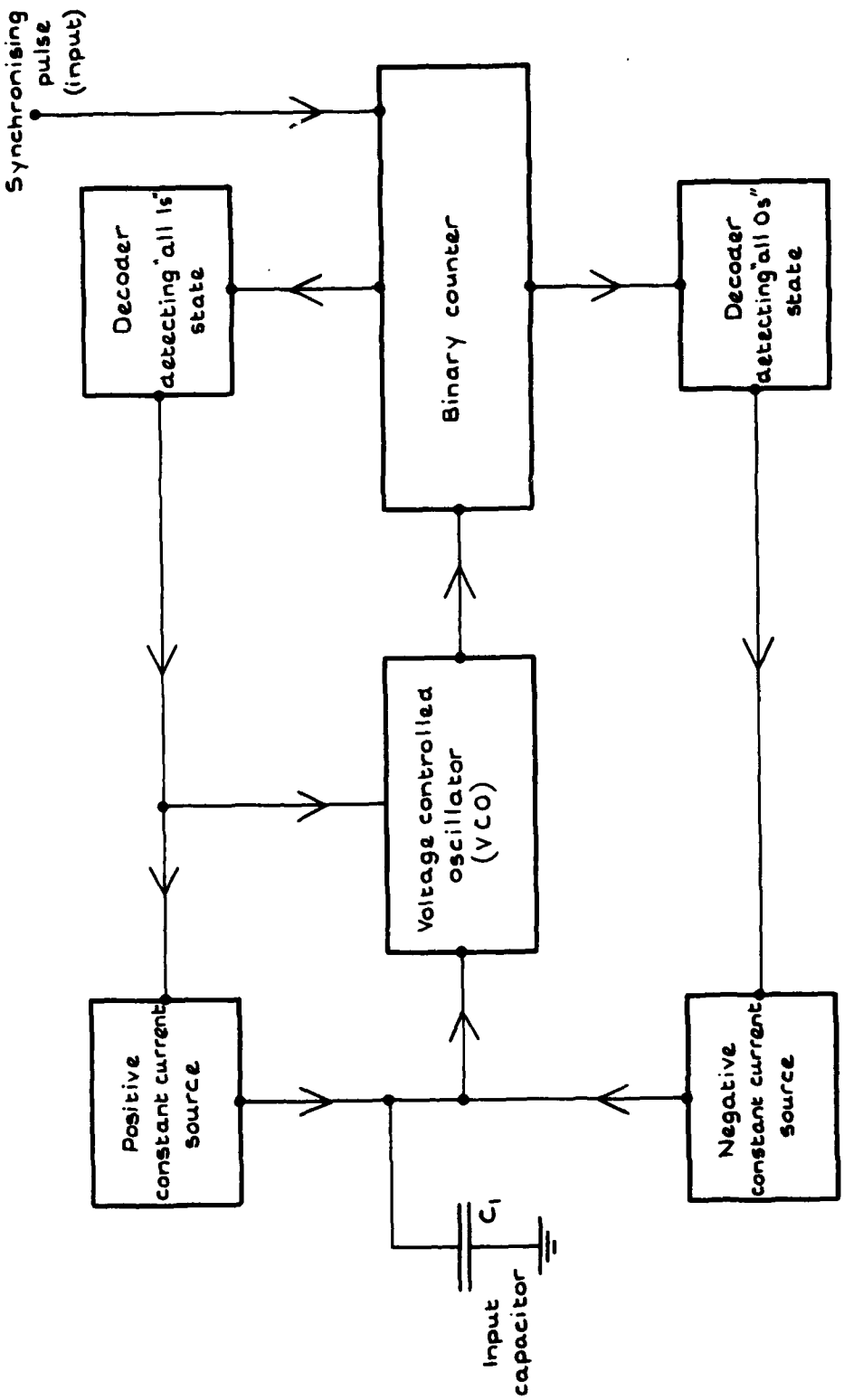

Fig 1 System block diagram

Fig 2a

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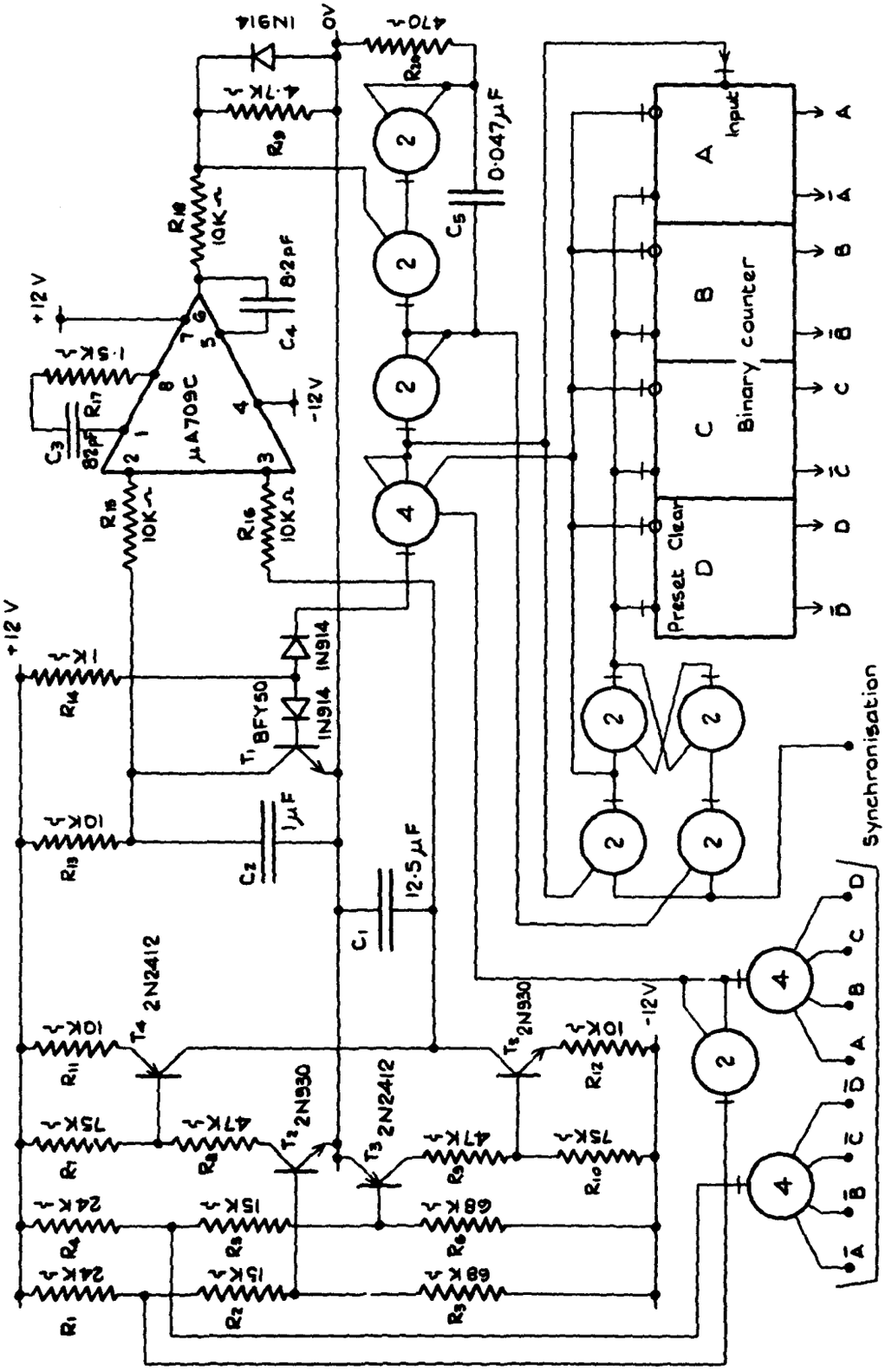

Fig. 2a Circuit diagram of system used in PCM simulator

Fig 2b

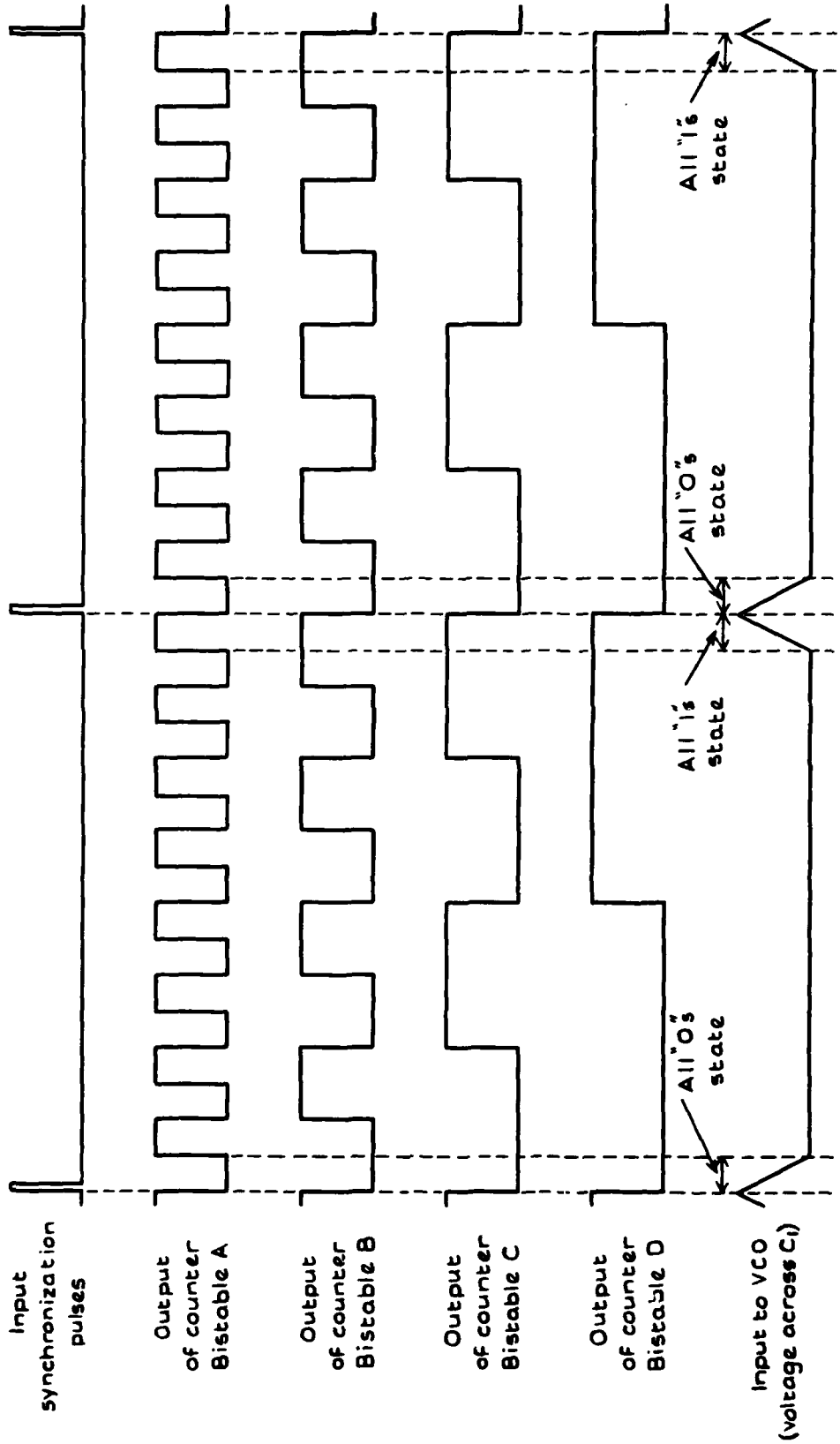

Fig. 2b Input and output waveforms

Fig. 3

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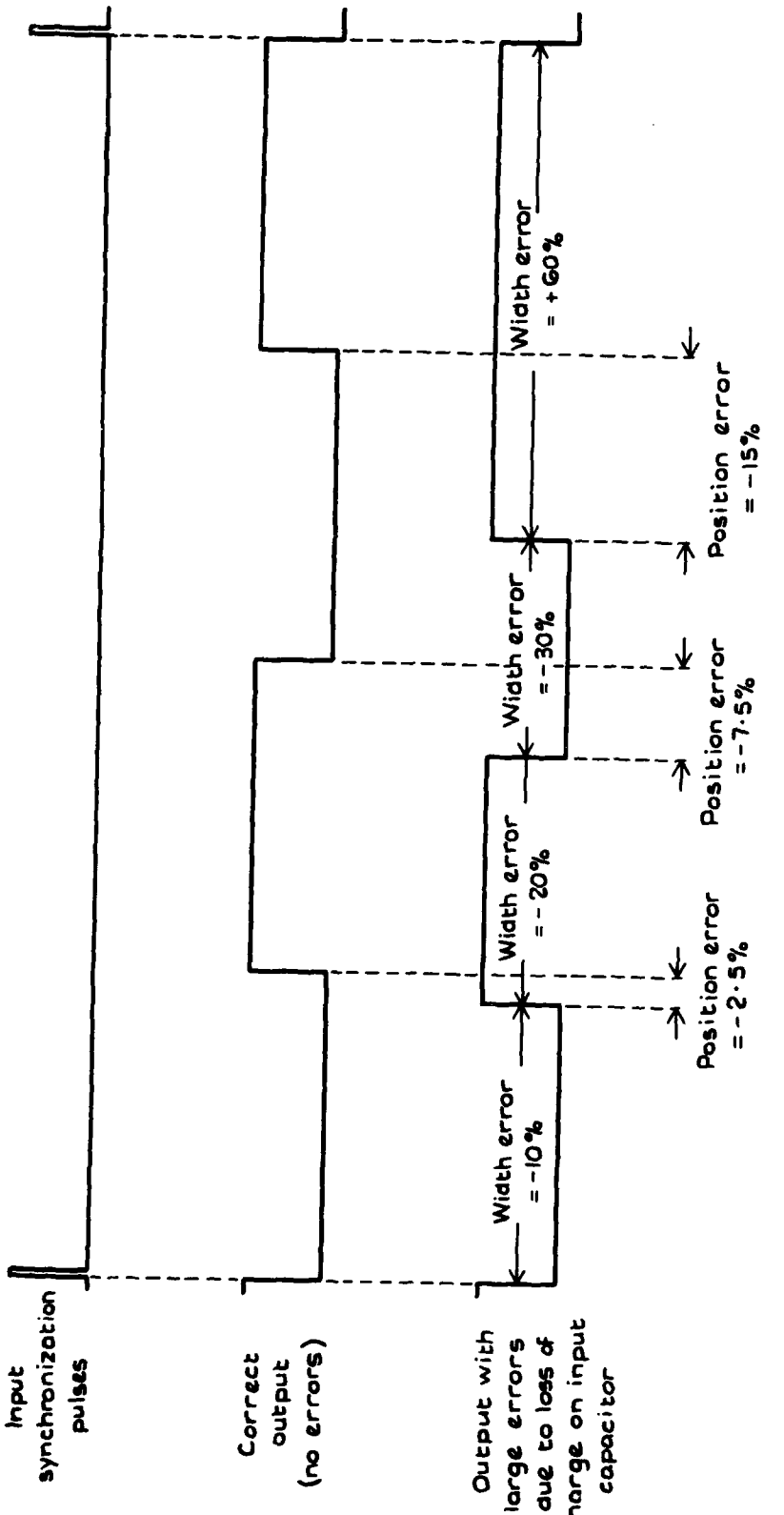
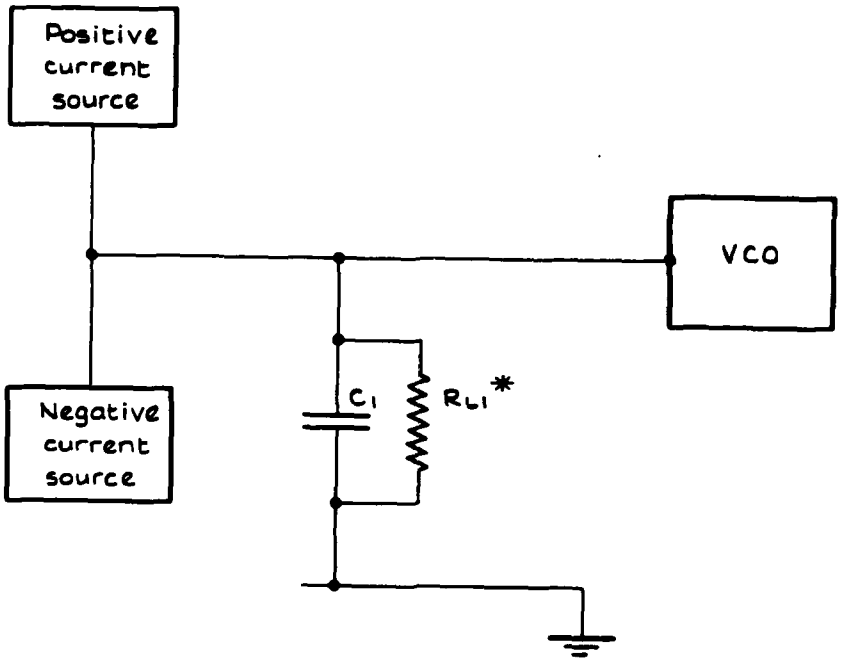
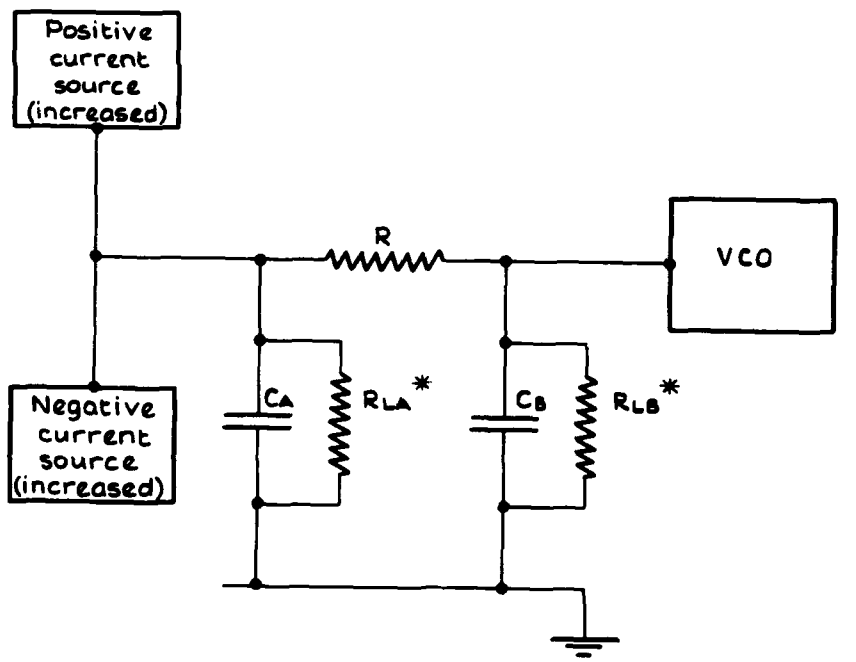


Fig 3 Effect of errors

Fig. 4a & b



a VCO input circuit before modification



b VCO input circuit after modification

* These represent the effective shunt resistances across the capacitors

Fig. 4a & b Modified VCO input circuit

Fig. 5

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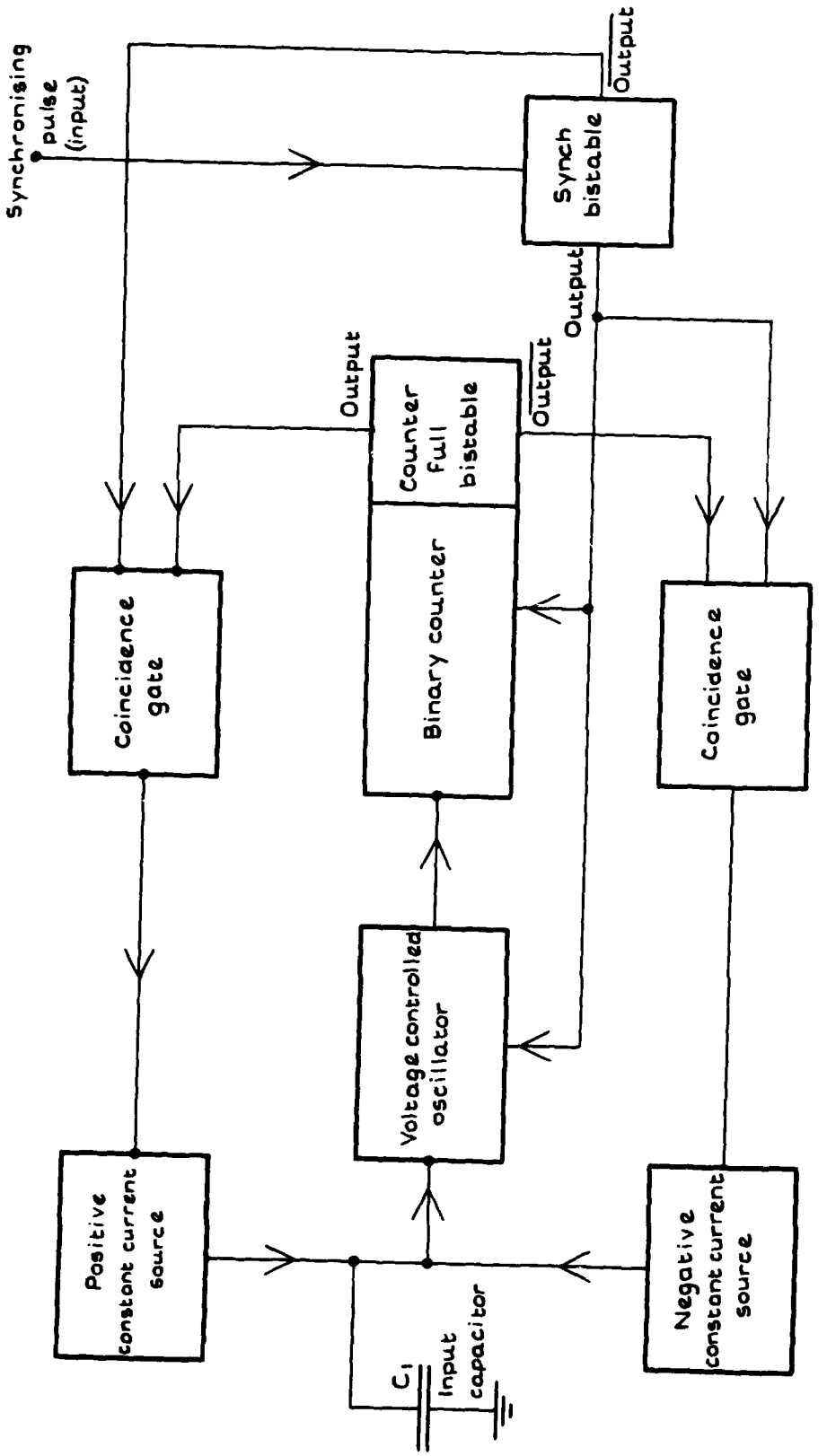
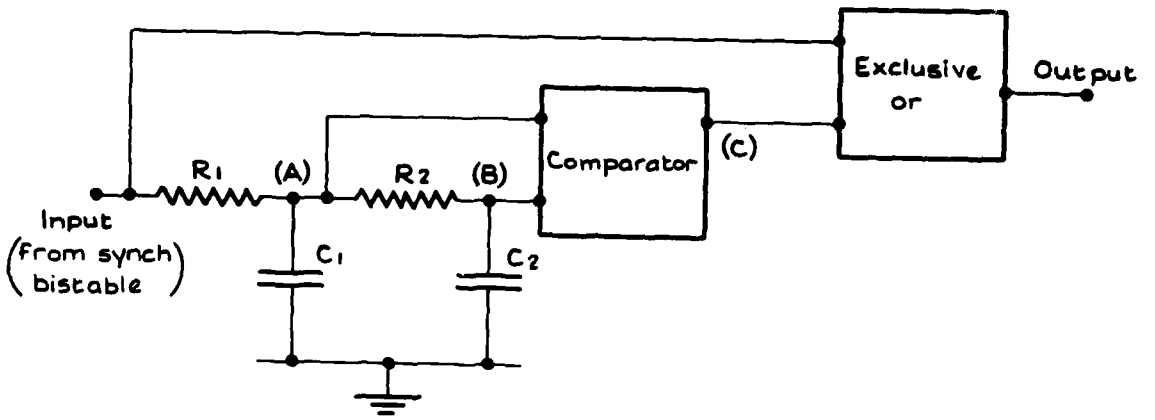


Fig. 5 Modified block diagram

Fig. 6



Circuit waveforms

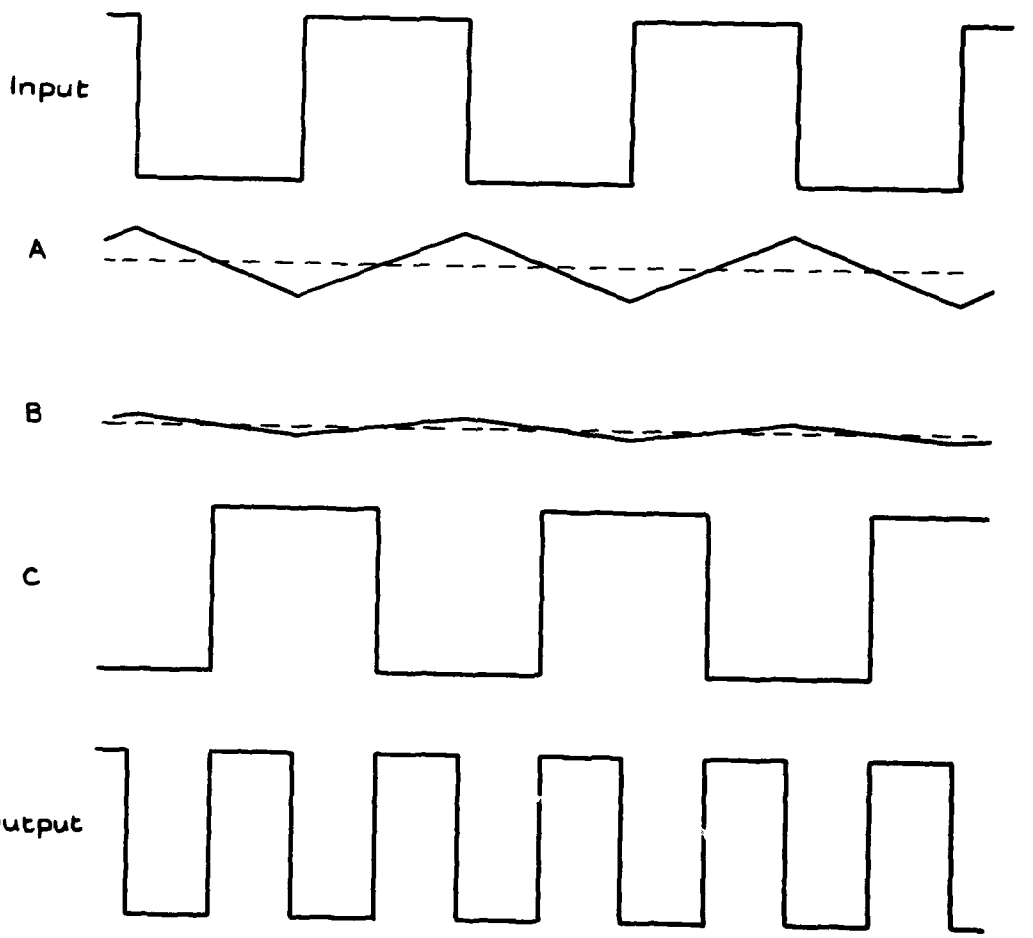


Fig. 6 Frequency doubling circuit